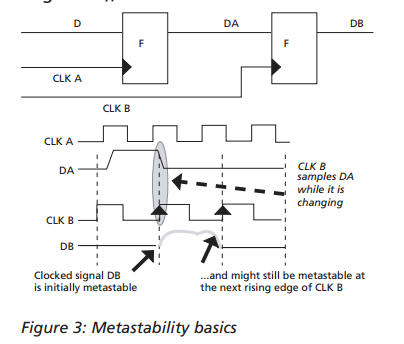
Q4 (a)(i) identify two scenarios in which clock domain crossing will be present in the FPGA

* Failures are not always repeated.
* EDA tools typically do not detect and flag these problems.
* Cross clock domain failure are difficult to detect and debug if they are not understood.
* Multiple clock domain within a window around the active clock edge as defined stup and hold time.

(ii) if these setup and hold-time requirements are not met, the output of the flip-flop may take much longer than tCO to reach a valid logic level. This is called unstable behavior, or metastability.

if CLK B samples DA while DA is changing (at the rising edge of CLK and falling edge of D), then DB will be metastable.

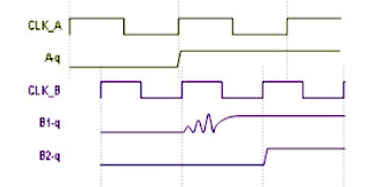
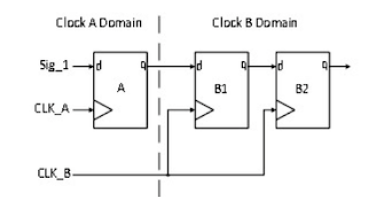


(iii)Double flopping

Is a technique that can be used when passing single bit signals between two asynchronous clock domains.

In general, a conventional two flip-flop synchronizer is used for synchronizing a single bit level signal., flip flop A and B1 are operating in asynchronous clock domain. There is probability that while sampling the input B1-d by flip flop B1 in CLK\_B clock domain, output B1-q may go into metastable state. But during the one clock cycle period of CLK\_B clock, output B1-q may settle to some stable value. Output of flop B2 can go to metastable if B1 does not settle to stable value during one clock cycle, but probability for B2 to be metastable for a complete destination clock cycle is very close to zero.

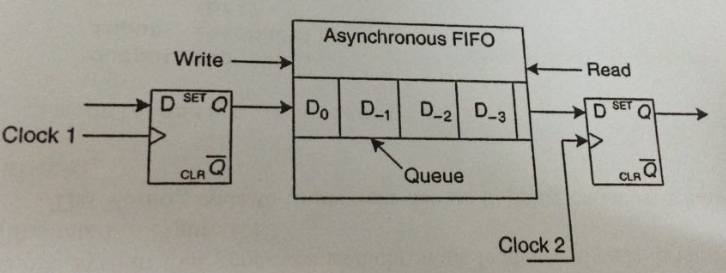
A greater number of flop stages may be used if frequency is too high as it will help in reducing the probability of synchronizer output to remain in metastable state.



FIFO structure

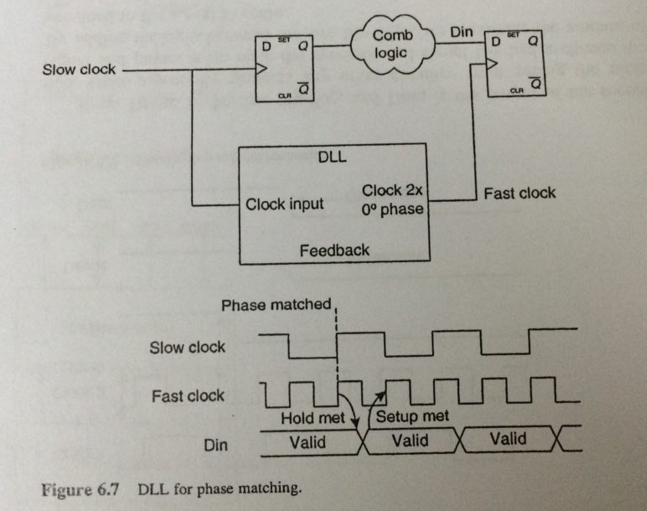
A more complicated way of passing data between clock domain is through FIFO.

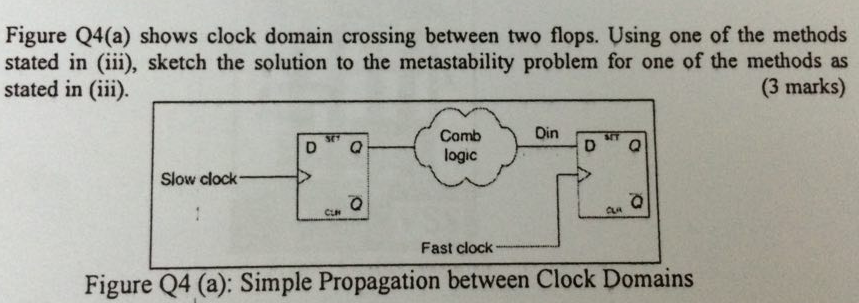
FIFO is best way to synchronize continuously changing vector data between two asynchronous clock domains. Asynchronous FIFO synchronizer offers solution for transferring vector signal across clock domain without risking metastability and coherency problems. In Asynchronous FIFO design, FIFO provides full synchronization independent of clock frequency.



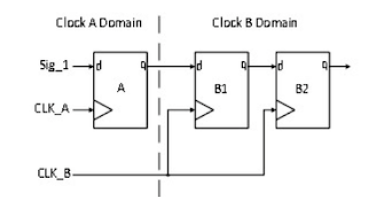
Phase control

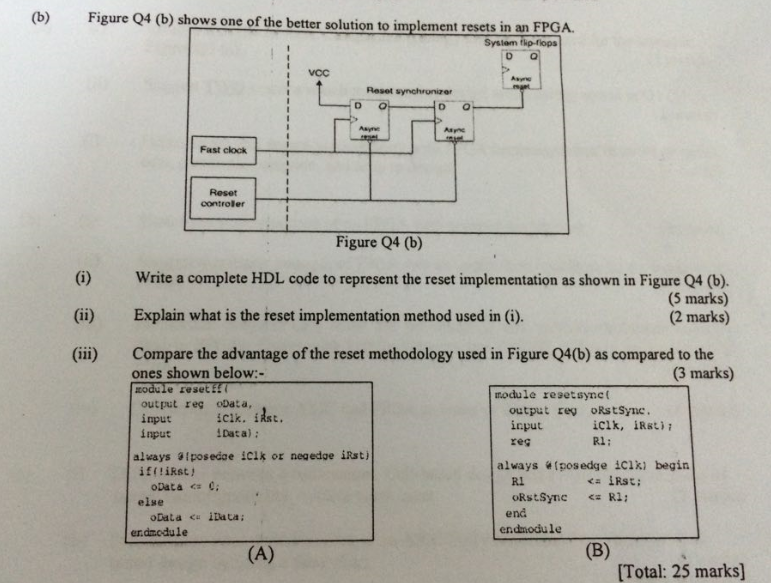
One of the clock via internal Phase Locked Loop (PLL) or Delay Locked Loop (DLL) and one of the clock has a period that is a multiple of the other within the resolution of the PLL or DLL then phase matching can be used to eliminate timing violation



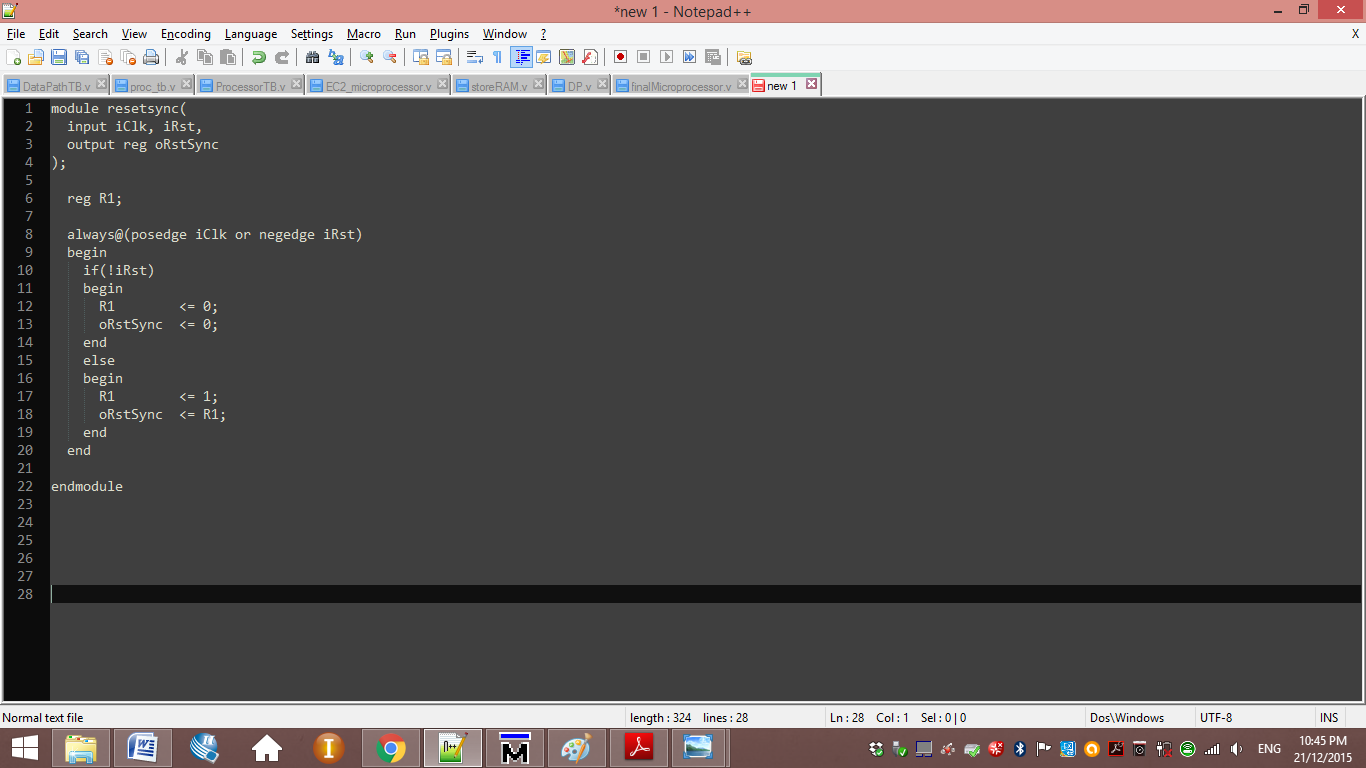
(iv) 

Solve with double flopping





(i)



(ii)

Allow the flip flop to be place into reset independent the clock but taken out the reset in synchronous with clock. Asynchronous assertion synchronous de-assertion method

(iii)

Figure (A) is the code for asynchronous reset. Reset controllers are typically interested in the voltage level they are monitor. Advantage assertion.

Figure (B) is the code for fully synchronous. Advantage is de-assertion.